# CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

**Department of Electrical and Computer Engineering**

# ECE 526L

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# LAB – 5: Modelling of a Schematic 8-bit Register

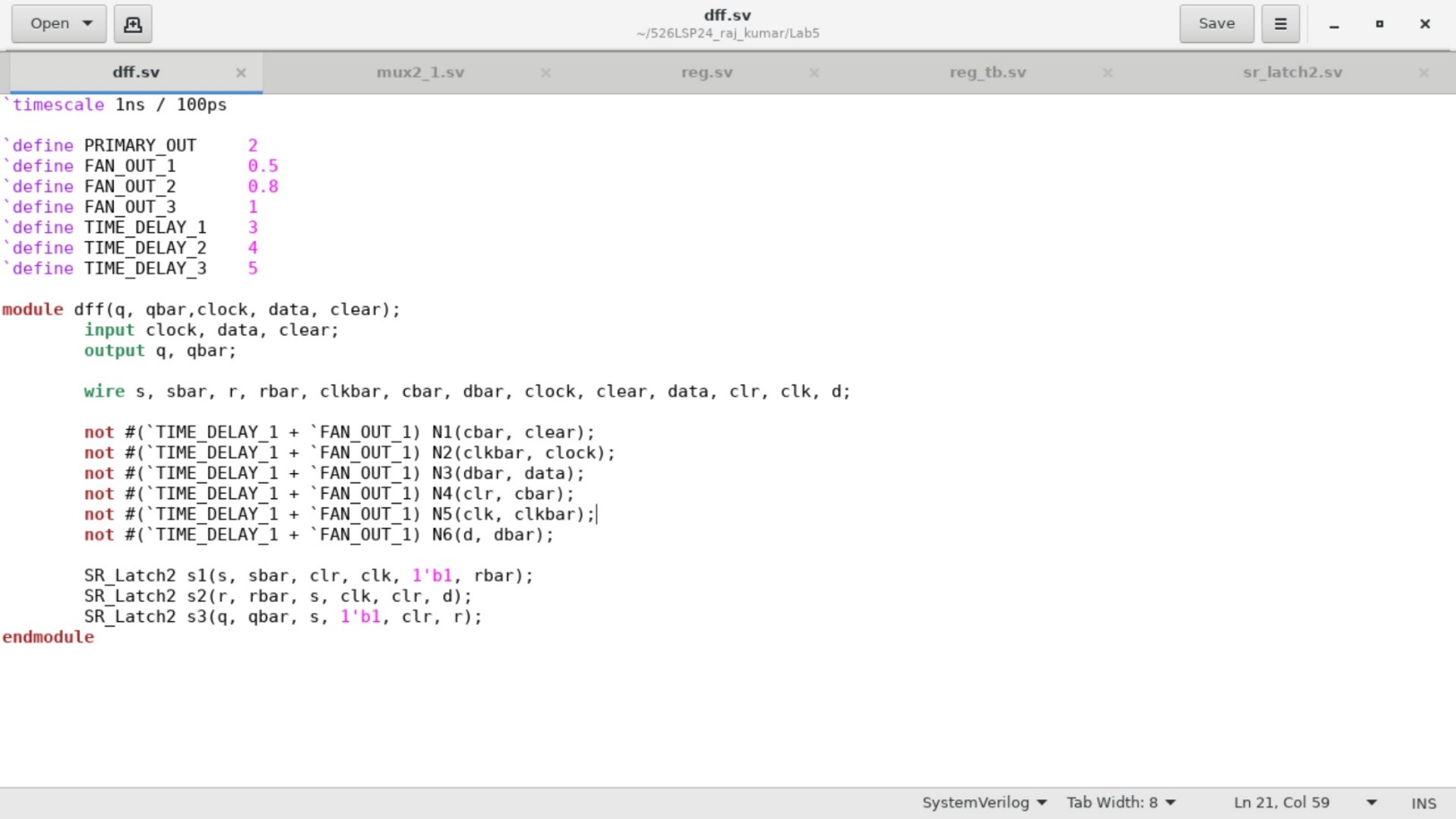
Written By: Raj Kumar

### Introduction: In this lab, we will know about 8-Bit Register using Synopsys VCS in Linux OS environment and different terminal commands

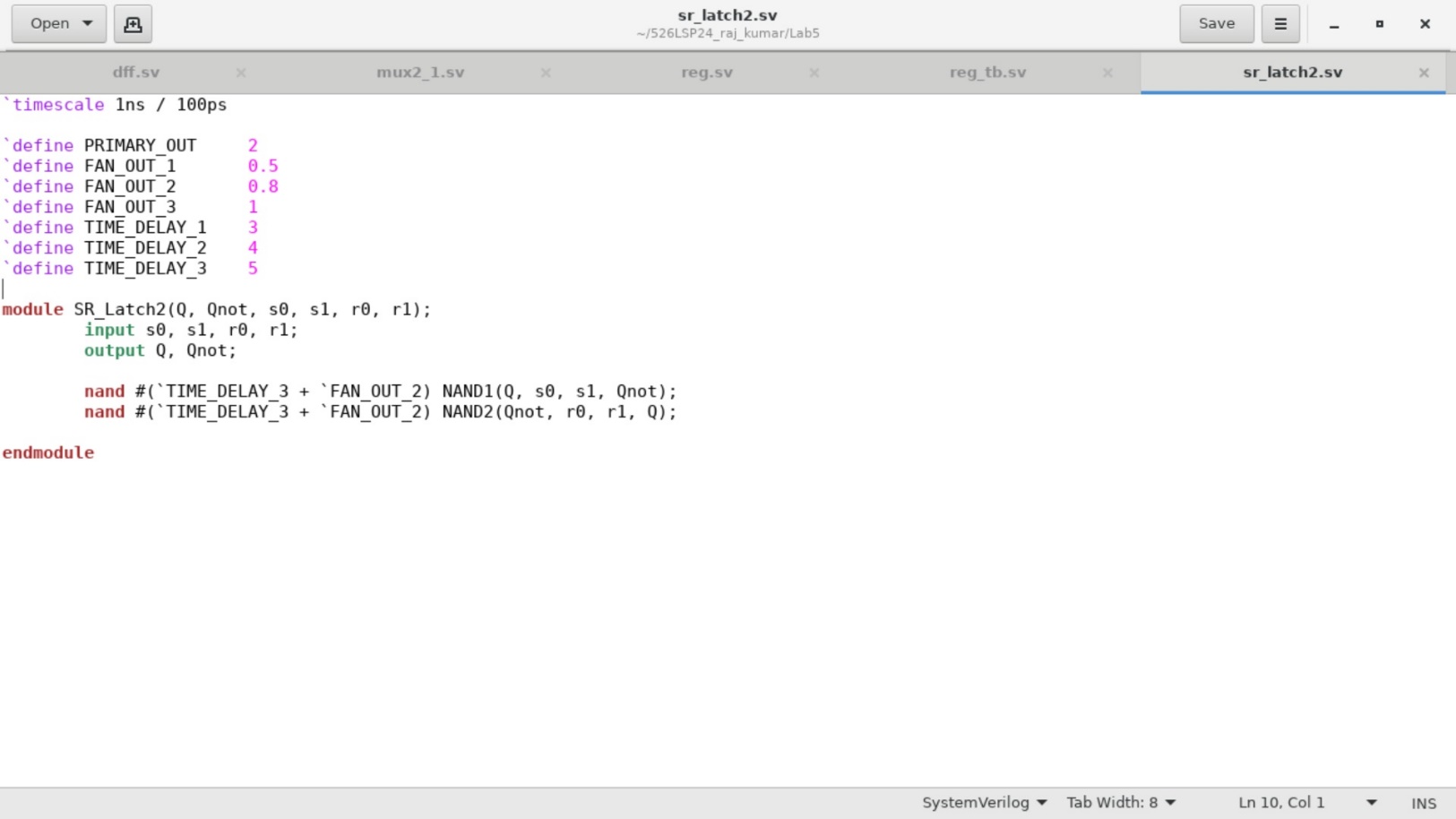
### Methodology: The first thing is being familiar with the Linux and Synopsys VCS that will navigate your system using terminal.

Use Linux based text editors with command line using,  
**“gedit”** and the file should have **“.v”** extension

Create a Verilog model of 8- bit register as given;

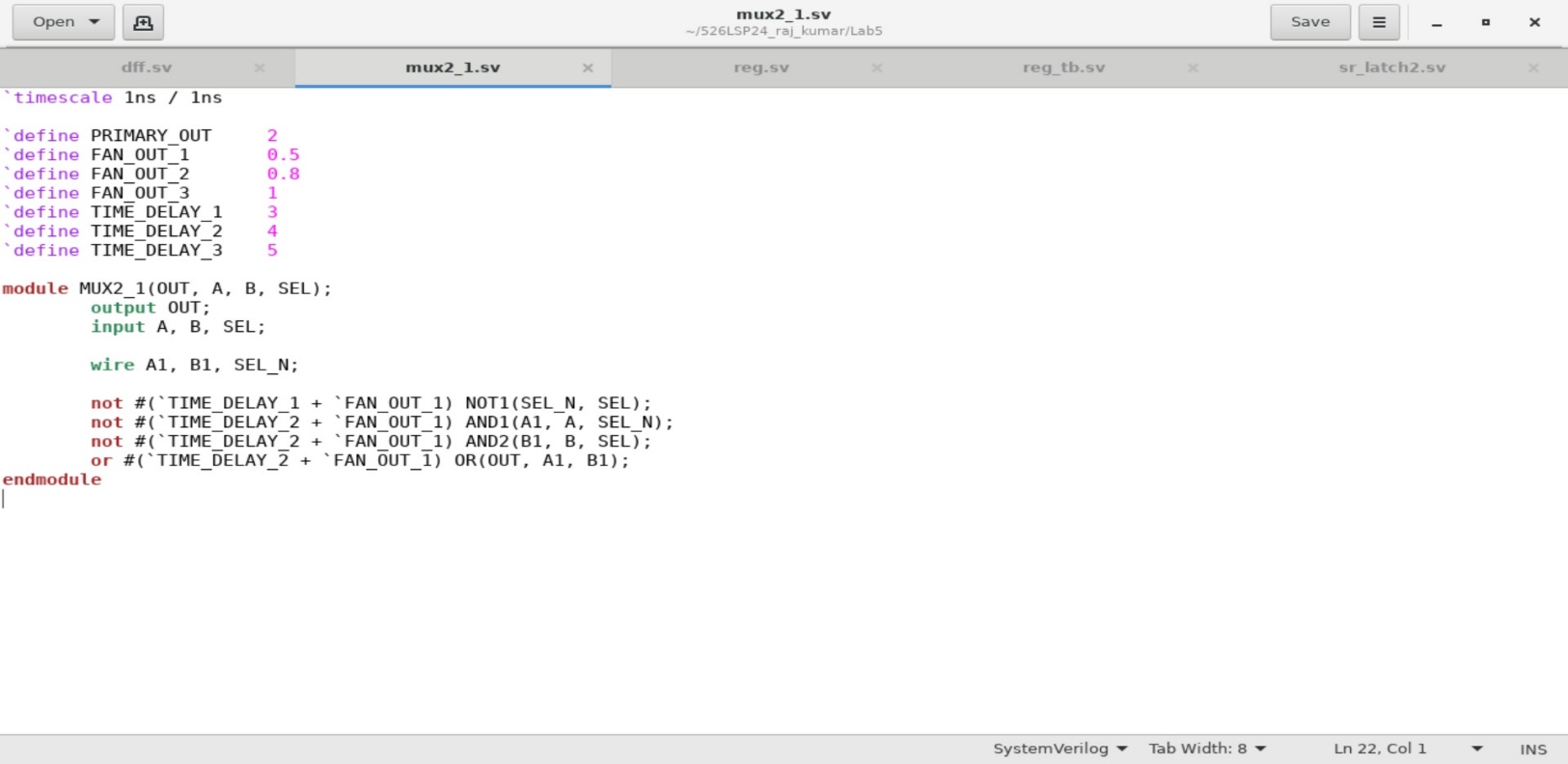


This is the fig of **“dff.sv”**, store it in new file, also in folder **“Lab5”**.

Now, the **sr\_latch2**: 

This is the fig of **“sr\_latch2.sv”** and save it and Lab5.

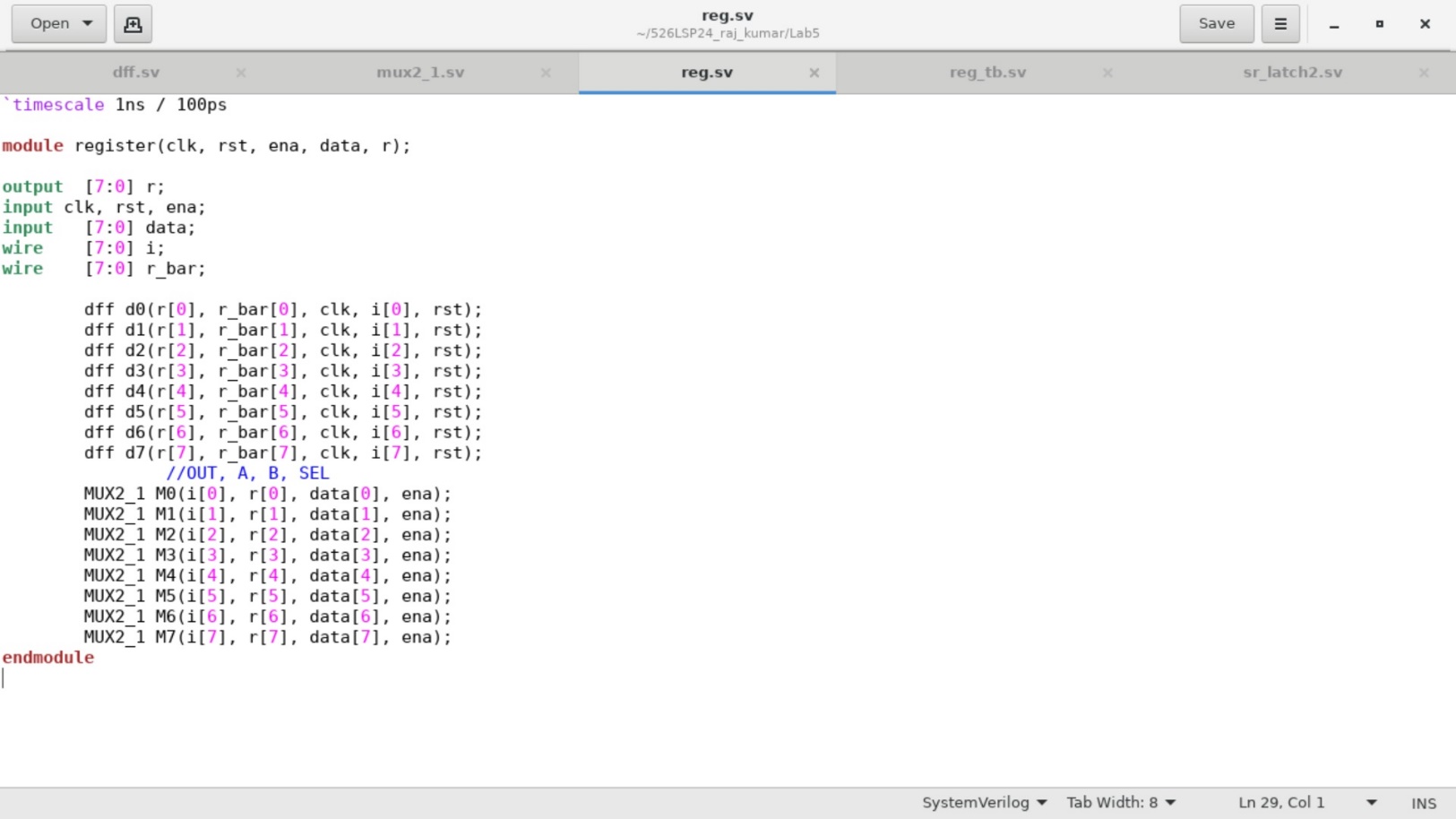
Now use the multiplexor model provided in the assignment and add the same gate delays for the multiplexor cells as used elsewhere from Lab4.



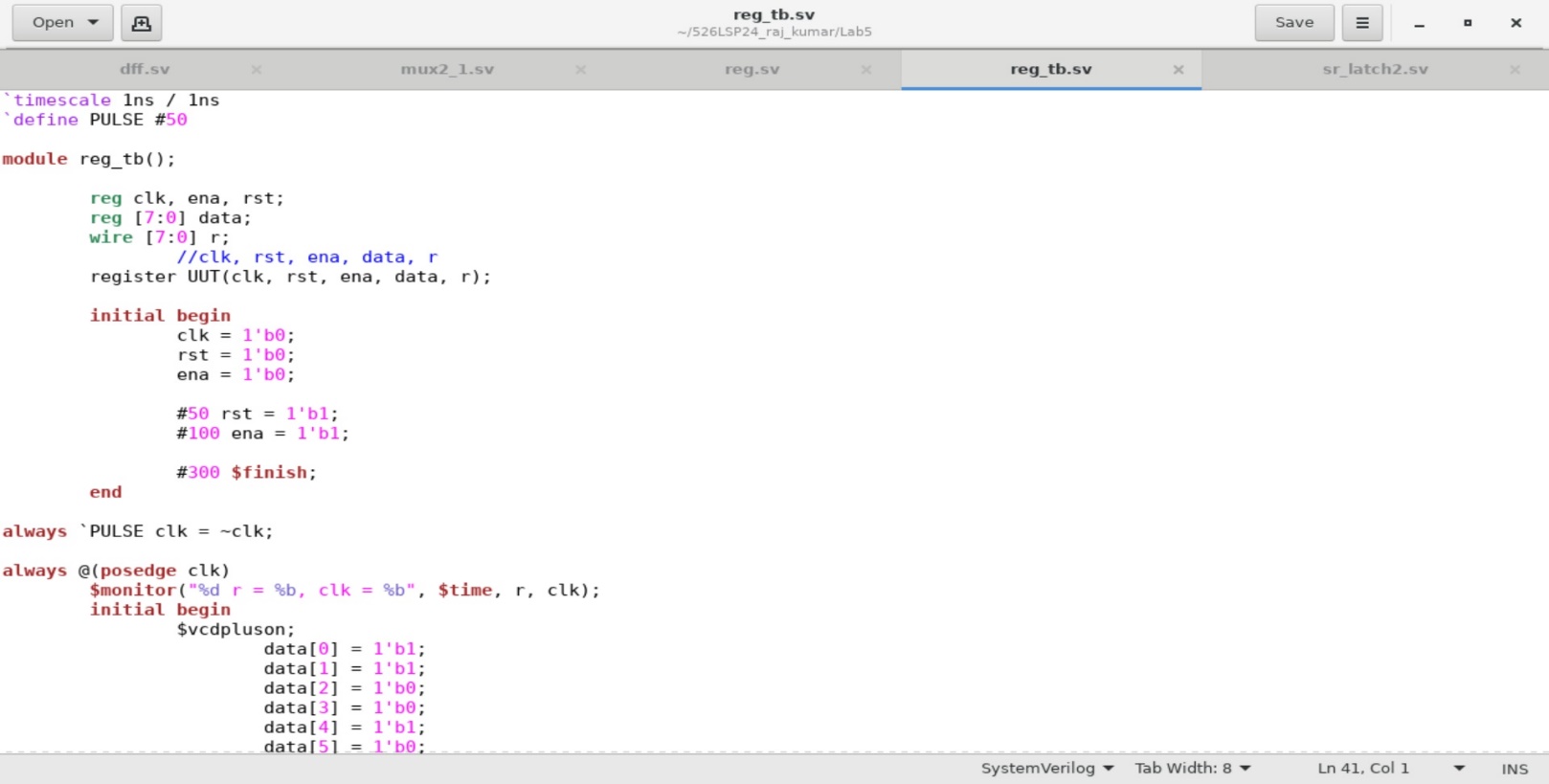
This is the fig of **“mux2\_1.v”** and save it in Lab5.

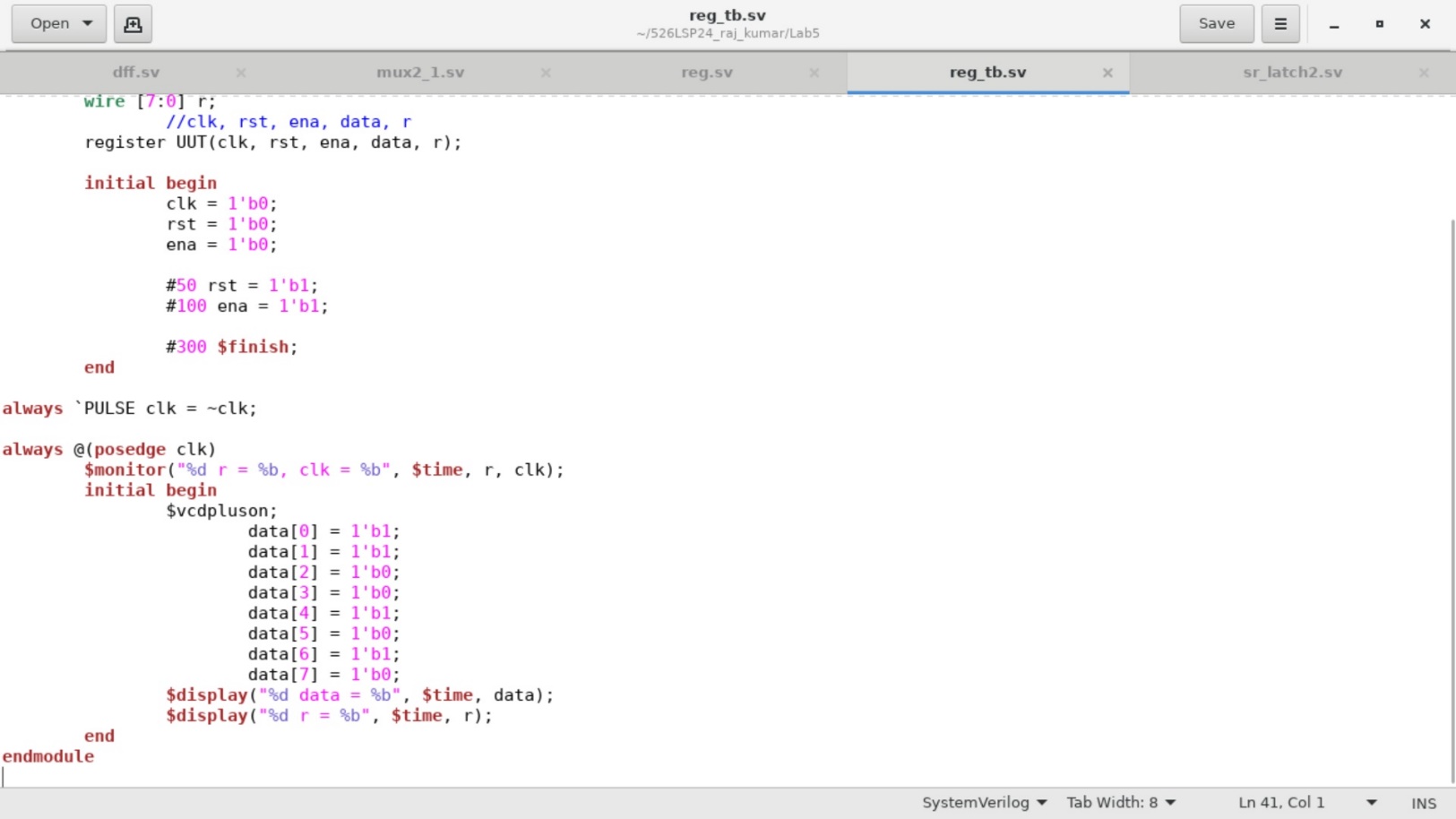
Now from the given assignment the register has the logic symbol, from its symbol the functions of the **registers “rst”** and **enable “ena”** can be inferred. use the following module header as given in the assignment and save it as **“reg.v”** and save it in **Lab5**.

The below figure is the design file of register;



Now, write a testbench module to verify the functionality of our design and save it as **“reg\_tb.v”**





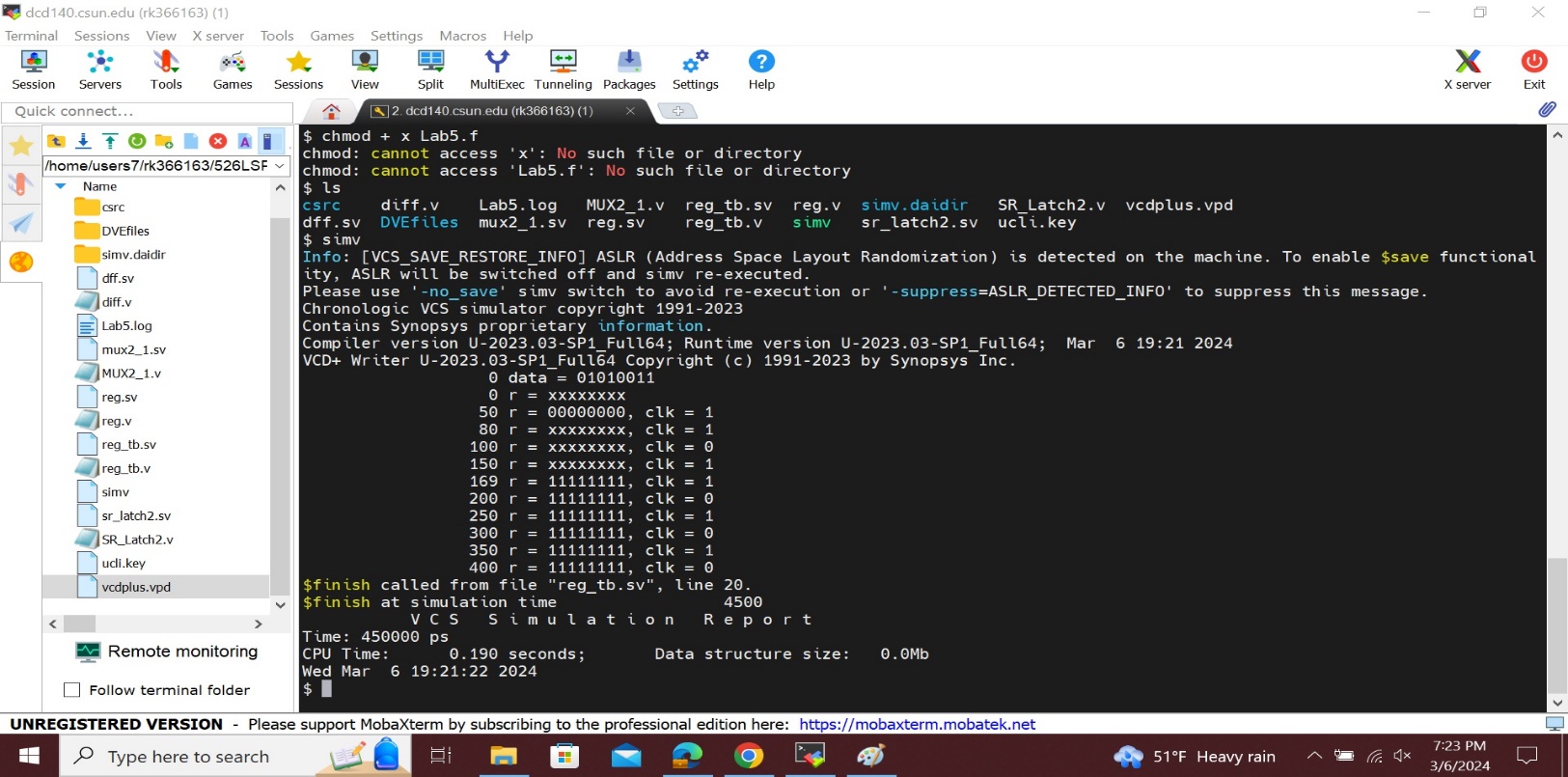
Now for compiling we should create a directory, write a command line code and name it as **lab5.f**

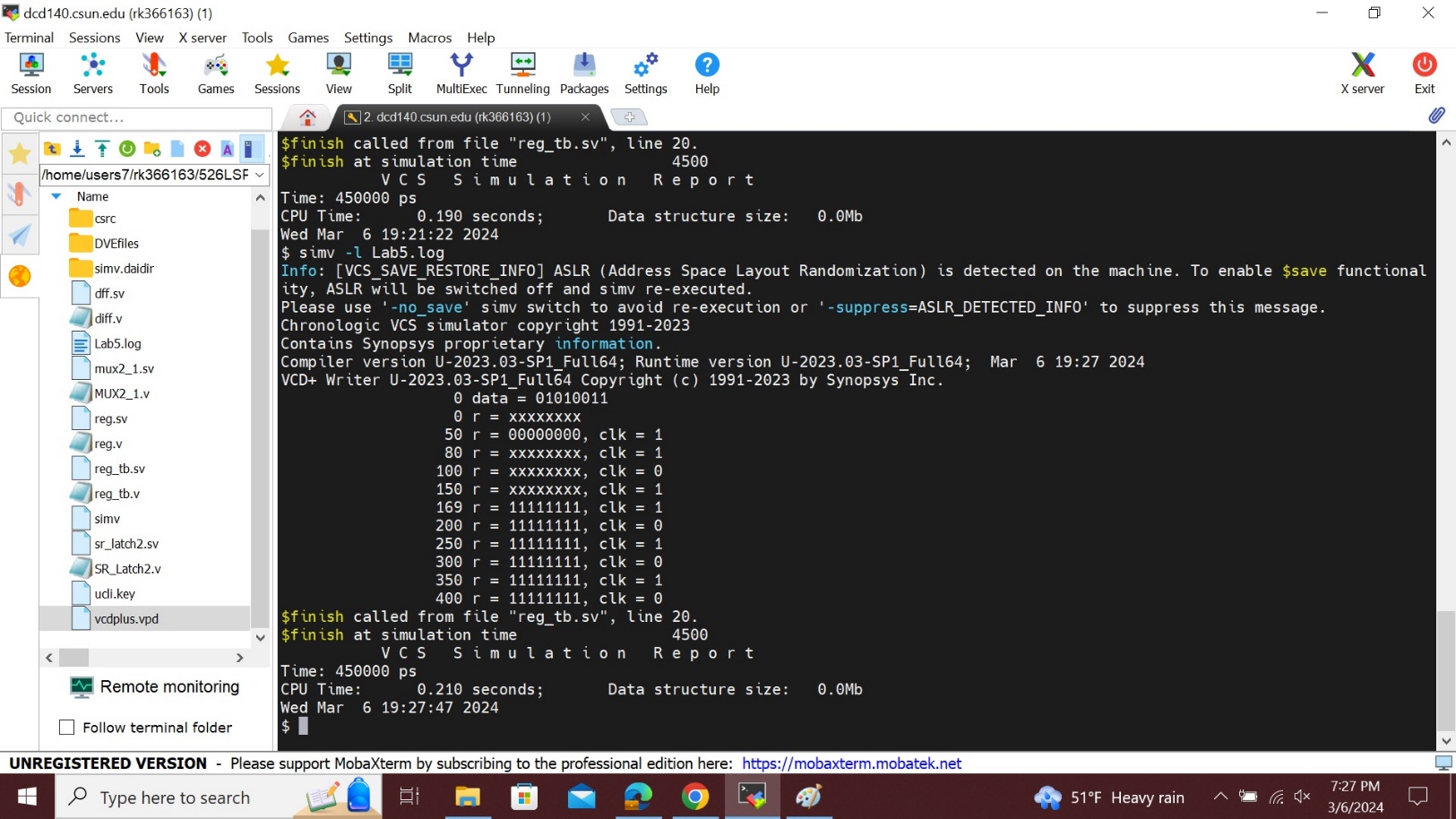
Use the command **“ls”** and then next use the command **“chmod +x lab5.f ”.**

Then use command,

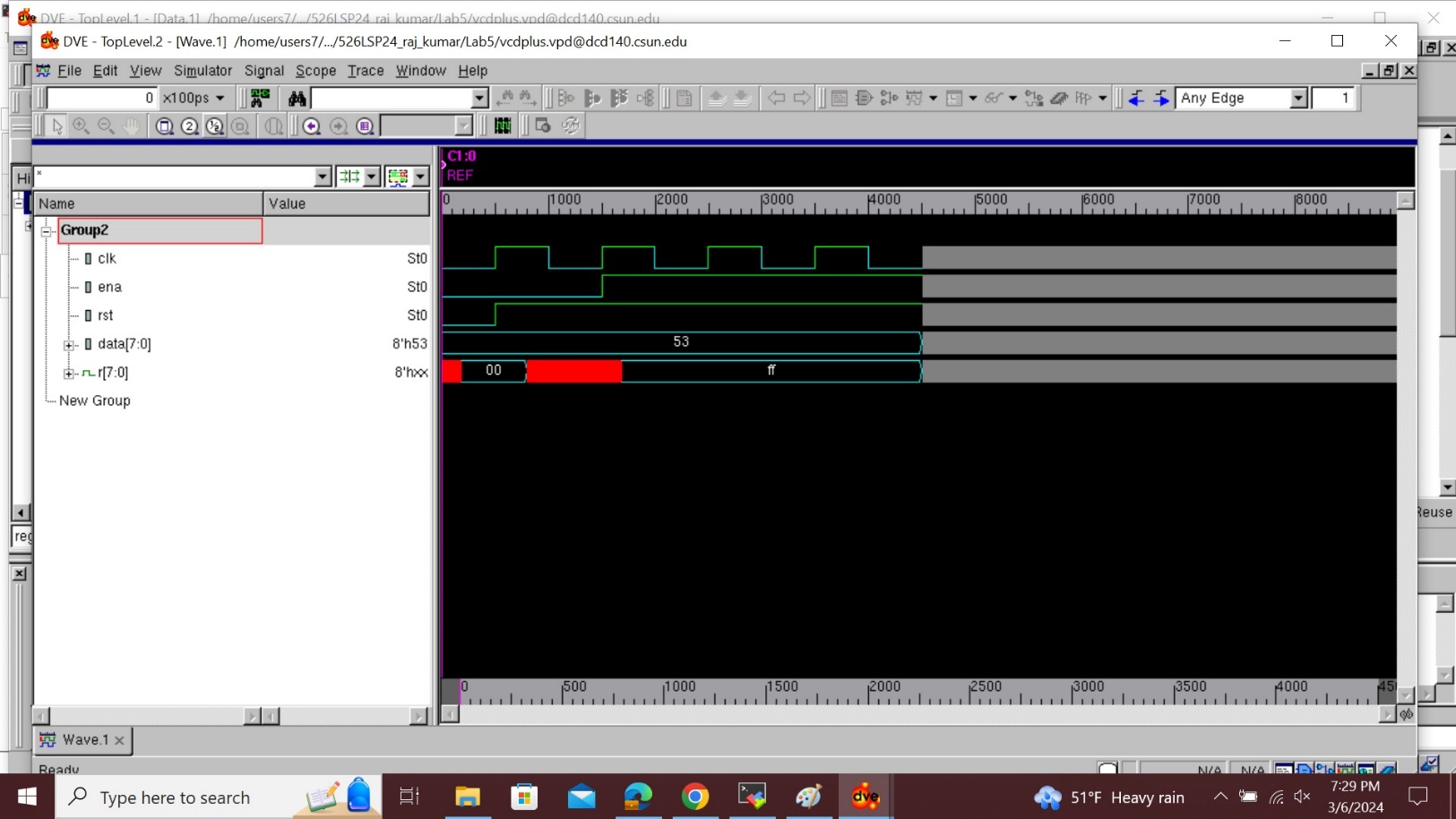
**“vcs -debug\_access+all -sverilog dff.sv mux2\_1.sv sr\_latch2.sv reg.sv reg\_tb.sv”**

**simv:**



**Log file:**To see the wave form first type **“dve”** command line then we will get the blank simulation window then go to file and open database then choose **vcdplus.vpd** and open the file.

Then finally select all the signals with the mouse ,then right click and select to **“add to wave->new wave view”.** Then we will get the waveform as shown in below figure,



This is the wave form of Schematic 8-bit register.

## Analysis of result:

## Data is stored using an 8-bit register with an 8-bit mux. When we provide the data from 0 to 7, which is represented as 8 bits, it is for the register that the multiplexer allotted to us. which functions as an on/off switch thanks to its one output, eight inputs, and three select pins. According to the provided data, the simv output contains the storage data from the multiplexer. The design code sets the cutoff frequency at 269 seconds. That was made very evident in the waveform "Dve" above. The enable input, reset, reg, and input data are used to generate the final output, which is shown as a clock with a 50% duty cycle.

**Conclusion:**

In this lab we completed schematic for 8 -bit register .

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, neither have I allowed nor I will let anyone to copy my work.

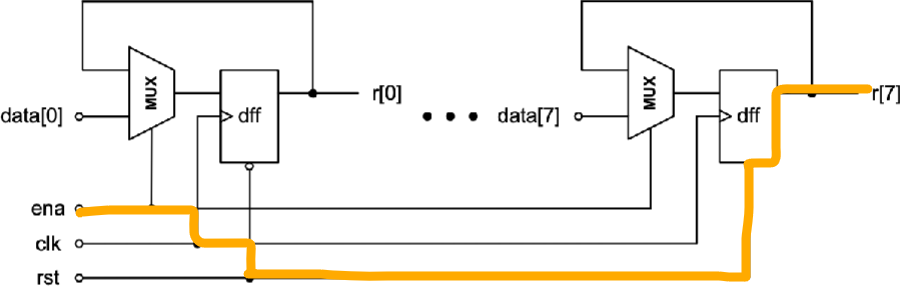
Name(printed) Raj Kumar

Name(signed) Raj Kumar

Date 03/07/2024

**LAB REPORT QUESTIONS**

## The longest path,



The calculation of longest path is;

= (3+0.5) +(3+o.8) + (3+0.8) + (3+2)

= 16.1 ns

## Maximum operating frequency range;

The formula for maximum operating frequency range is 1/f,  
i.e ~(1 /16.1) = 0.062MHz.